

Serial No.: <b>10/796,426</b>	Confirmation No.: 1895	Art Unit: 2183
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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Inventors:	<b>Brian Robert Prasky</b>	Date:	<b>12 June 2009</b>
Serial No.:	<b>10/796,426</b>	Art Unit:	<b>2183</b>
Filing Date:	<b>9 March 2004</b>	Examiner:	<b>Brian P. Johnson</b>
Confirmation No.	<b>1895</b>	Docket No.	<b>POU920030068US1</b>
Title:	<b>Method, System and Program Product for a Pipelined Processor Having a Branch Target Buffer (BTB) Table with a Recent Entry Queue in Parallel with the BTB Table</b>	Attorney:	<b>Graham S. Jones, II 42 Barnard Avenue Poughkeepsie, NY 12603-5023</b>

**AMENDMENT**

**The Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450**

**Your Honor:**

**In response to the Office Action of March 13, 2009, please amend the above-identified application as follows:**

<b>Amendments to the Specification begin</b>	<b>on page 2 of this paper.</b>
<b>Amendments to the Claims begin</b>	<b>on page 7 of this paper.</b>
<b>Remarks/Arguments begin</b>	<b>on page 13 of this paper.</b>